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SINGLE-EVENT UPSET TESTING OF THE PERFORMANCE SEMICONDUCTOR 1750A CMOS/SOS CHIP SET

JAMES D. KINNISON

THE JOHNS HOPKINS UNIVERSITY ■ APPLIED PHYSICS LABORATORY

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Complex computer systems in space are vulnerable to many different environmental effects. One of the most difficult problems is survival under exposure to charged-particle radiation. Microelectronic devices are particularly sensitive to single-event upset—a change in the logic state of a dynamic node or memory cell due to interaction with cosmic rays. For reliable computing in satellite systems, designers must understand the sensitivity of the computer components to single-event upset. A description of tests performed on a MIL-STD 1750A compliant microprocessor and peripherals is presented, and the results are used to estimate the single-event upset rate in space for each of the devices.

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ABSTRACT

Complex computer systems in space are vulnerable to many different environmental effects. One of the most difficult problems is survival under exposure to charged-particle radiation. Microelectronic devices are particularly sensitive to single-event upset—a change in the logic state of a dynamic node or memory cell due to interaction with cosmic rays. For reliable computing in satellite systems, designers must understand the sensitivity of the computer components to single-event upset. A description of tests performed on a MIL-STD 1750A compliant microprocessor and peripherals is presented, and the results are used to estimate the single-event upset rate in space for each of the devices.

CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

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1. INTRODUCTION

Complex computers have become commonplace in spacecraft systems. The demand for sophisticated on-board data processing and analysis cannot be satisfied with older, more established technology. In addition, many satellites are designed to perform autonomously; large sequences of commands are stored by the satellite and are executed without interaction with human operators. Each of these applications requires a reliable, high-performance computer system able to withstand the orbital environment.

For many satellite systems, the radiation environment due to naturally occurring charged particles is the most severe problem. These particles include electrons and protons trapped in the Earth's magnetic field, protons and heavy ions produced in solar events, and energetic heavy ions found in cosmic rays. A charged particle passing through a semiconductor device loses energy by ionizing the semiconductor material or by nuclear interaction. This energy loss causes a variety of effects in integrated circuits, which may be separated into two categories: cumulative effects and single-event effects.

Cumulative effects are those in which a single ionizing particle causes some local change in the semiconductor material without directly affecting the device performance. However, when many of these interactions take place, the overall device characteristics change. For instance, the creation of a single carrier trap in an integrated circuit oxide causes a small increase in the leakage current of a device, but millions of these traps can render a device unusable. These effects are often called total dose damage, or ionization damage, and are characterized by measuring the changes in a device as a function of total dose, in rads.

Single-event effects are those in which a single particle causes a global change in the integrated circuit. The two most common effects in integrated circuits are single-event upset and latch-up. Single-event upset occurs when an ionizing particle creates enough electrons in a small region to change the state of a memory cell. Information stored in a bit or group of bits is lost; without some error detection scheme, we can never be sure that a computer program or data have not been corrupted. Ionizing particles can also introduce enough charge in certain types of complementary metal oxide semiconductor (CMOS) devices to cause a short circuit from the device power supply to ground through the device substrate. This current is usually more than the integrated circuit can safely carry, and thus the device is destroyed.

To reduce the sensitivity of computers to the charged-particle environment in space, several different radiation-hardened technologies have been developed for the construction of computer components. In particular, integrated circuits made using silicon-on-sapphire (SOS) technology are inherently immune to latch-up, and are much less sensitive to single-event upset than identical devices built using standard CMOS or epitaxial CMOS technology. In addition, the processes used to build SOS integrated circuits can be adjusted so that the resulting devices are more resistant to total dose damage.

This report documents tests performed to measure the single-event susceptibility of a hardened MIL-STD 1750A chip set used in mission critical satellite computer applications. The chip set was designed by Performance Semiconductor and fabricated by Westinghouse using CMOS/SOS wafers hardened to withstand up to 100 krads (Si) without significant degradation.

2. THE SPACE ENVIRONMENT

The charged-particle environment near the Earth is dominated by effects due to the geomagnetic field. Therefore, the problem of radiation effects in space can be separated into two cases: the interplanetary environment and the near-Earth environment. The particle types and energies are different for these two cases, and the methods used to measure and prevent radiation effects depend on which environment will dominate the mission. We will concentrate here on the near-Earth environment.

2.1 Galactic Cosmic Rays

Galactic cosmic rays are primarily composed of highly energetic ions of the natural elements. An empirical model of the ion flux spectrum for each element as a function of energy is available. Although energy spectra are useful, a more convenient parameter for characterizing the ion flux is the linear energy transfer (LET), which is defined as the rate at which energy is deposited in a material by an ion

along its path. To first order, the LET of an ion is equivalent to the ion stopping power, or dE/dx, in the target material. The energy spectra can be converted to LET spectra by using

$$f(S) = f(E)\frac{dE}{dS} \tag{1}$$

where f is ion flux, S is LET, and E is particle energy. This is the form most commonly used in radiation effects calculations.[1]

The Earth's magnetic field interacts with cosmic rays and solar protons. The strength of this interaction depends on the charge-to-mass ratio of the incident ion and is characterized by the magnetic rigidity, $\Re$, defined as

$$\Re = cBR = \frac{pc}{Ze} \tag{2}$$

where B is the magnetic field strength, R is the gyroradius of the particle around the field line, p is the momentum, c is the speed of light, and Ze is the charge of the ion.[2] The trajectory of particles with a given magnetic rigidity can be traced backwards. Some of these orbits will intersect the Earth, and some will remain confined to the vicinity of the Earth. These are "forbidden" trajectories, and the particle flux for these trajectories is zero. For cosmic rays, with relatively constant flux during the Earth's rotation, a particle's rigidity completely determines whether it is in a forbidden or an allowed trajectory. Thus, the Earth's magnetic field provides some shielding against cosmic rays, especially for low-inclination orbits.

2.2 Solar Protons

Protons produced in solar events can also cause significant damage to satellite systems. An epochal analysis of the annual proton flux produced in solar events over the solar cycle shows that the cycle can be divided into two periods: four inactive years of low annual fluence and seven years with annual fluence greater and 5×10^7 protons/cm^2 (>10 MeV). The active period extends from two years before solar maximum to four years after maximum. The times of solar maximum for the 19th through 22nd cycles are 1957.9, 1968.9, 1979.9, and 1990.9, respectively.

The distribution of solar proton fluence has been modeled. The four inactive years at solar minimum have such low fluences that they are not considered in the model. The active years are best modeled with a log normal distribution such that the probability of exceeding a given fluence f_p over a mission of length t is

$$P(f > f_p, t) = \sum_{n=1}^{\infty} p(n, wt)Q(F, n) \tag{3}$$

where f_p is written as 10^F, F is distributed normally, and $p(n, wt)$ is the probability of n events occurring during mission length t if an average of w events occurred during the observation period. This probability is assumed to follow a Poisson distribution:

$$p(n, wt) = e^{-wt}\frac{(wt)^n}{n!} \tag{4}$$

$Q(F, n)$ is the probability that the sum of all fluences due to n events will exceed 10^F. The values for $Q(F, n)$ have been evaluated numerically using Monte Carlo techniques. The results of this simulation can then be used to calculate $P(f, t)$.[3]

2.3 Trapped Protons and Electrons

Charged particles in a dipole magnetic field experience three distinct quasi-periodic motions: gyration around the field lines, bounce between conjugate mirror points, and azimuthal drift around the dipole. The net effect of these motions is to trap the particles in belts around the Earth. These particles are the dominant source of total dose degradation in low-Earth orbit.

Empirical models of the radiation belts have been compiled from satellite measurements made over the last three decades. These are presented as tables of time-averaged omnidirectional proton and electron fluxes as a function of energy and position in magnetic field coordinates. The most recent of these are AP-8 for protons and AE-8 for electrons. These models do not include short-term variations, diurnal variations, or other time-depen-

[1] J. H. Adams, Jr., Cosmic Ray Effects on Microelectronics, MR 5901, Naval Research Laboratory, Washington, D.C. (Dec 1986).

[2] J. H. Adams, Jr., "The Variability of Single Event Upset Rates in the Natural Environment," *IEEE Trans. Nucl. Sci.* 30, 4475-4480 (1983).

[3] J. Feynman and S. Gabriel, "A New Model for Calculation and Prediction of Solar Proton Fluences," in *Proc. 28th Aerospace Sciences Meeting*, American Institute of Aeronautics and Astronautics, Reno, Nev. (8-11 Jan 1990).

dent effects; the data only reflect the behavior of the radiation belts averaged over periods longer than one year.

AP-8 gives fluxes for protons with energy between 0.1 and 400 MeV.[4] The spatial and energy distributions of the belts are changed by solar activity, so two versions of the model are provided—one for solar minimum conditions, the other for solar maximum. The peak flux corresponds to the proton belt, which occurs at an altitude of about 4500 km in the equatorial plane. Electron models for solar minimum and maximum conditions are given in AE-8 (J. I. Vette, private communication). These models give the omnidirectional electron flux for particles with energy between 0.25 and 7 MeV. As with the protons, belt-like structure is observed, but in this case, two regions of high concentration are present. The higher flux region nearer to the Earth is called the inner zone and peaks at an altitude of about 4500 km; the belt further from the Earth is the outer zone, which peaks at about 23,000 km. The region of lower flux between the inner and outer electron belts is called the "slot" region.

2.4 South Atlantic Anomaly

Anomalies exist in the spatial distribution of the trapped particles around the Earth. The most important of these for spacecraft operations is the South Atlantic Anomaly. Because the center of the Earth's magnetic field is displaced from the geographic center, the magnetic field is weaker over the southern Atlantic Ocean than anywhere else at the same altitude. Therefore, the charged particles in the Earth's magnetic field encounter their lowest mirror point in this region. The effect is to produce anomalously large particle flux over this region. For satellites in low-Earth orbit that pass through this region below 1000 km, the total dose environment is dominated by particles in the South Atlantic Anomaly.[5]

3. SINGLE-EVENT EFFECTS

A heavy ion traveling through an integrated circuit generates electron-hole pairs along the path of the particle by ionization. If the particle track passes through a sensitive region in a storage element of an integrated circuit, enough electrons may be collected to cause the element to change state. This effect is known as single-event upset and occurs most often in memory devices such as static random access memory (RAM). However, any device that includes latches, counters, registers, or similar structures may be susceptible to single-event upset. An ion must pass through a sensitive region to cause upset; any other particle path will not.

For a monoenergetic beam of ions with linear energy transfer L, the sensitivity of the device to upset is characterized by the parameter σ, called the upset cross section:

$$\sigma = \frac{N}{\Psi} \tag{5}$$

where N is the number of errors generated by exposure to a beam fluence Ψ. The probability that a particle traveling through a device will cause an upset is the ratio of the cross section to the total active area of the integrated circuit. The cross section is measured for particles with a range of LETs. This cross-sectional curve can then be combined with any heavy-ion spectrum to generate an estimate of the error rate for that device in the orbit with a given heavy-ion spectrum.

4. DEVICE DESCRIPTIONS

The Performance Semiconductor 1750A chip set implements the MIL-STD 1750A instruction set architecture, a high-performance architecture used in many high-reliability computer systems. The chip set consists of a central processing unit (CPU), a processor interface circuit (PIC), and a memory management unit (MMU). All three devices were fabricated using a Westinghouse process by which commercial CMOS integrated circuit designs are con-

[4] D. M. Sawyer and J. I. Vette, *AP-8 Trapped Proton Environment for Solar Maximum and Solar Minimum*, NSSDC/WDC-A-R&S. National Science Data Center, Greenbelt, Md. (1976).

[5] W. N. Spjeldvik and C. G. Rothwell, "The Radiation Belts," in *The Handbook of Geophysics and the Space Environment*, A. S. Jursa, ed., AFGL-TR-85-0315, Air Force Geophysics Laboratory, Hanscom AFB, Mass., pp. 5-1 to 5-55 (1985).

verted to SOS designs. The resulting devices have transistors with 1-μm gate lengths and 250-Å oxides.

4.1 PACE1750A CPU

The PACE1750A is a general-purpose 16-bit microprocessor designed for high-performance floating-point and integer arithmetic. The processor provides an instruction set with 130 instruction types and a large variety of data types. Instruction types include comprehensive integer arithmetic, floating-point arithmetic, data-type conversion, stack manipulations, and loop controls. Memory access is provided via 13 different addressing modes for a total address space of up to 2 MWords of segmented memory (in 64-kWord segments, where a Word is 2 bytes).

Physically, the processor includes 16 general-purpose registers, 8 other user-accessible registers, and an array of real-time application-support resources. These include programmable timers, an interrupt controller supporting 16 levels of interrupts ranked by priority, and a fault handler controlling internally and externally generated faults. The processor uses a multiplexed 16-bit bus for external communication.

At a clock frequency of 40 MHz, the processor achieves a throughput of 2.6 million instructions per second (MIPS) for the DAIS instruction mix, which is a standard real-time integer and floating-point instruction mix used to compare instruction throughput in microprocessors. Integer addition operations are executed in 0.1 μs, whereas integer multiplication operations are executed in 0.575 μs. Similarly, floating-point addition requires 0.7 μs, whereas floating-point multiplication requires 1.075 μs.

4.2 PACE1753 COMBO

The PACE1753 is a support device for the PACE1750A microprocessor that contains a memory management unit and a block protection unit. Functionally, the device provides memory management and access protection for up to 1 MWords of memory. In addition, up to 1 MWords of memory may be write-protected in pages of 1 kWord each. The device also detects illegal input/output accesses or access to unimplemented blocks of memory, as defined by MIL-STD 1750A. Error correction on the data bus is included as well; single-bit errors on the data bus are corrected, and double errors are detected. Finally, the PACE1753 acts as a bus arbitrator for up to four masters on a fixed priority basis determined by hardware interconnection.

4.3 PACE1754 PIC

The PACE1754 is a PIC used to provide support functions for the PACE1750A microprocessor. In a typical MIL-STD 1750A implementation, the functions provided by the PIC are generated by discrete components. The PACE1754 integrates these functions into one device, thus increasing the performance of the computer.

The PIC functions are programmable, and the desired configuration is stored in a control register on the device. Possible functions include programmable system watchdog timers, clock outputs for additional peripheral devices, programmable bus time-out detection, and built-in system test functions.

5. TEST METHODOLOGY

The single-event upset cross section of a device is measured by exposing it to a beam of heavy ions with known LET, operating the device in some test circuit, and counting the number of errors produced. The particle beams needed can only be produced at a small number of accelerator laboratories around the world. One of the most commonly used U.S. facilities is the Tandem Van de Graaff generator at Brookhaven National Laboratory. In general, several beams are used to measure the cross section as a function of LET.

Single-event upset tests come in two varieties: static and dynamic. Static tests are performed by loading a series of bits into a device, exposing the device to a beam, and then counting the errors after the exposure. Memory devices are usually tested in this fashion. Dynamic tests are performed by actively exercising a device during exposure to the particle beam and continuously checking for errors. These tests are usually performed on microprocessors and other dynamic devices.

Interfacing test equipment to devices is a difficult problem. The ions used in single-event upset testing interact easily with air. Therefore, the sample devices must be exposed in a vacuum chamber. This requirement places severe restrictions on test equipment; it must either reside in the vacuum chamber with the test sample, or it must pass data through vacuum feed-throughs. Commercially avail-

able test equipment is not suited to the vacuum environment, since it may be too large to fit in the chamber or dissipate too much power to operate under the thermal constraints of a vacuum. Operating a sample device through feed-throughs is also difficult. The cables used to interconnect the sample device and the test equipment become quite long—several meters or more—and sample devices may not be able to drive such long cables. In addition, long cables are more sensitive to electrical noise.

The configuration used to test the PACE1750A chip set is given in Figure 1. The FORTH reduced instruction set computer (FRISC) was mounted in the vacuum chamber with the 1750 computer to reduce interface difficulties. In addition, all the computers used in the experiment used RS-232 serial ports to communicate with each other. The only exception to this was the external reset line added to allow the FRISC computer to force a reset of the 1750 computer in the event that an ion caused the 1750 computer to stop functioning. An iris was used to reduce the beam spot diameter to irradiate one device. Each chip in the PACE1750A chip set was individually irradiated by moving each device into the beam. Therefore, any errors observed were due solely to upsets in the irradiated device. Beam control and characterization were provided by the Brookhaven staff.

5.1 FRISC Test Computer

The FRISC computer is based on a 32-bit reduced instruction set computer (RISC) microprocessor, called the FRISC microcontroller, which runs programs written in FORTH. FRISC was designed at APL for use in embedded microcontroller applications. The core of the single-event upset test computer is a single-board computer made by Silicon Composers and built around the FRISC. We have added several special circuits that allow direct control of sample devices in a heavy-ion beam, as well as diagnostic information to determine the health of the sample and computer. These blocks are as follows:

1. Parallel Card—allows a device to be mapped directly into the memory space of the FRISC. Inputs to the device are supplied by writing to its address; outputs are examined by reading the address.
2. Serial Card—allows a system to communicate with the FRISC via an RS-232 or RS-485 serial connection. This mode is used to test microprocessors mounted in a single-board computer running some test software.
3. Analog Card—monitors system and sample supply voltage, supply current, and temperature. Since many devices that are sensitive to single-event upset are

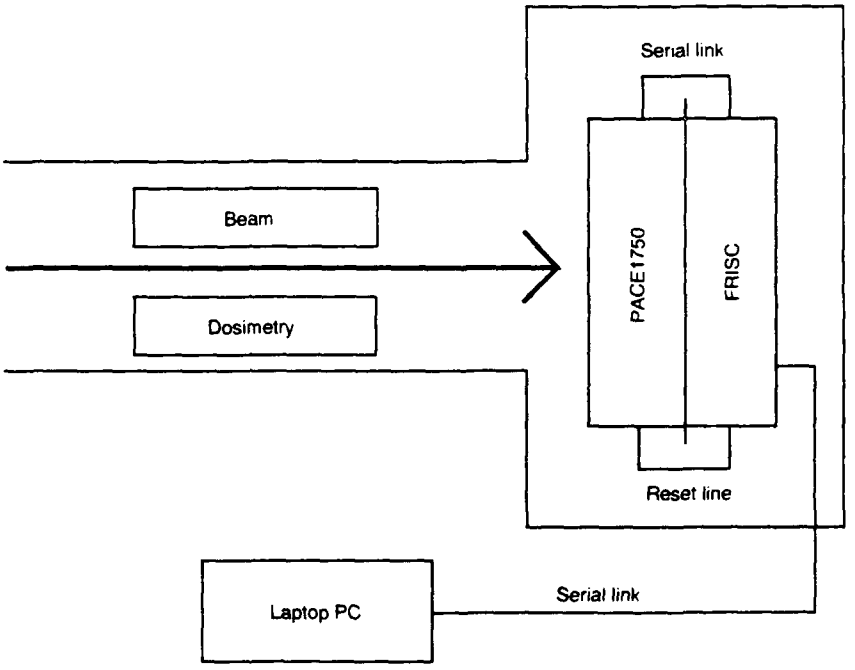

Figure 1 Diagram of the PACE1750A single-event upset test hardware.

also sensitive to latch-up, a latch-up detection and protection circuit is included. This circuit allows investigation of the electrical characteristics of a latched device without destroying the sample.

This computer configuration is compact and dissipates less than 7 W, and so can be used in a vacuum chamber without the difficulties inherent in commercial test equipment. In addition, the interface to sample devices is modular, so tests of new device types can be developed rapidly. Each of the devices discussed below was tested using this computer system.[6]

5.2 1750 Test Computer

The PACE1750A chip set was exercised using an engineering model of a spacecraft attitude processor designed at APL. This board is a stand-alone computer system containing read-only memory (ROM) for boot-up, RAM for program execution, and several serial and parallel ports for data transfer and external communication. The program run during the experiment was executed from ROM. As mentioned earlier, a signal line was added to provide a way to reset the 1750 computer in the event that an error disturbed the communication between the 1750 computer and the FRISC computer.

The 1750 test code used in the experiment consisted of a sequence of operations that exercised all three devices that make up the 1750 chip set; the same program was used no matter which device was irradiated. An outline of the program is as follows:

1. Fill the COMBO lookup tables with a known bit pattern.
2. Test the PIC configuration registers for upset.
3. Load the CPU registers with test data.
4. Perform a series of arithmetic operations.
5. Perform a series of logical functions.
6. Test the CPU registers for errors.
7. Test the MMU lookup tables for errors.

Each dynamic operation was performed twice, and the results were compared for errors. After each step, a status character was sent to the FRISC computer. If an error occurred, the 1750 computer reset itself.

In some cases an upset can cause a microprocessor to stop functioning. In the tests described here, the PIC was used as a watchdog timer for the CPU. If the CPU failed to reset the PIC timer in the allotted time, a reset was forced, and an error logged. In addition, if the status character was not received by the FRISC computer in a timely fashion, the 1750 computer was reset, and an error logged.

6. RESULTS

Two samples of the CPU and COMBO, and a single sample of the PIC were tested. The beams used in this experiment are given, along with LET and range in silicon, in Table 1. Range and LET variation effects are important in interpreting test data. As a particle passes through a material, it loses energy. At the end of its range, the LET of a particle increases rapidly. For the relatively low-energy particles produced by accelerators, the range is on the order of 10 to 500 μm in silicon. If an incident particle is stopped near the sensitive regions of a device, the LET of the

Table 1
Ions used in the PACE1750 test.

Ion	Energy (MeV)	Beam LET (MeV·cm^2/mg)	Range in Si (μm)	Average flux ($\times 10^4$ p/cm^2·s)
^{79}Au	290	78.9	28.9	2.5
^{35}Br	260	37.7	34.5	2.0
^{28}Ni	265	26.6	45.2	2.0
^{17}Cl	206	11.2	60.3	2.5

[6] J. D. Kinnison, R. H. Maurer, P. L. McKerracher, and B. G. Carkhuff, "A Summary of Recent VLSI SEU and Latchup Testing," *Proc. 1992 IEEE Radiation Effects Data Workshop*, New Orleans (14 Jul 1992).

particle is not the nominal beam LET; a correction for the change in LET must be made when plotting this data point. For CMOS/SOS devices, the active regions are all within 10 μm of the surface, and ions with ranges beyond the active region are easily generated.

Each of the samples was delidded and exposed individually to the beams. The FRISC computer counted errors, monitored device supply voltage and current, and measured device case temperature. No anomalous voltages, currents, or temperatures were observed.

The average cross section for each device type as a function of LET is given in Figure 2. Recent research has shown that the cross section is well represented by an integral Weibull distribution, given by

$$\sigma(L) = \sigma_0 \left[1 - e^{-\left(\frac{L - L_0}{W}\right)^s} \right] \qquad (6)$$

where L is LET ($L > L_0$), L_0 is the threshold LET, and σ_0 is the asymptotic cross section.[7] The remaining parameters, W and s, determine the shape of the distribution. Table 2 gives parameters for a maximum-likelihood estimation of the distributions for each of the device types. The Weibull functions may be used in combination with any cosmic ray spectrum to calculate the upset rate for that exposure.

The most sensitive device type is clearly the COMBO, which has the lowest threshold and highest cross section (per device). However, when the cross section of each device is scaled by the number of bits exercised, the asymptotic cross sections are all about 5×10^{-8} cm^2/bit. This result compares well with tests performed on other CMOS/SOS devices.

The upset rate in an Adams 90% worst-case cosmic ray environment is often used to compare the relative sensitivi-

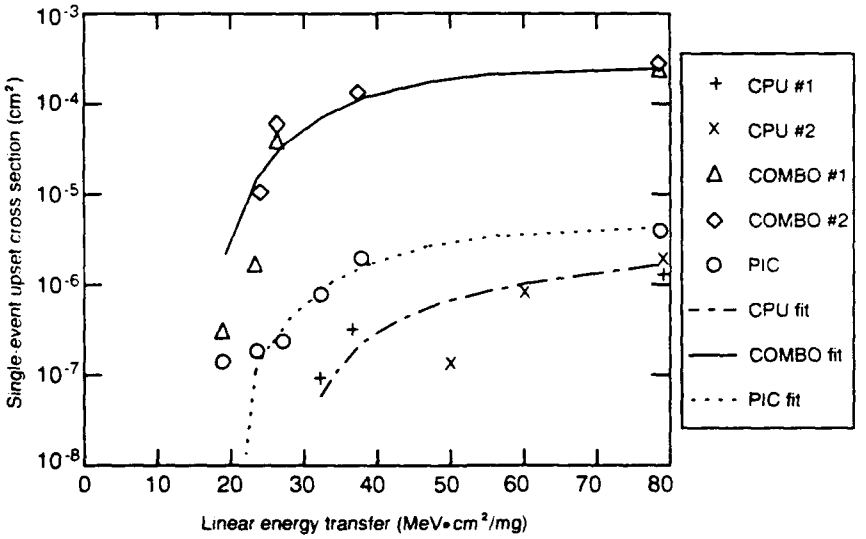

Figure 2 Single-event upset cross sections for the PACE1750A chip set.

Table 2
Weibull parameters for each device.

Device	σ_0 (cm^2)	L_0 (MeV·cm^2/mg)	W (MeV·cm^2/mg)	s
CPU	3.5×10^{-6}	29.0	65	1.3
PIC	4.5×10^{-6}	18.9	28	1.9
COMBO	2.5×10^{-4}	16.5	27	2.0

[7] E. L. Petersen, J. C. Pickel, J. H. Adams, Jr., and E. C. Smith, "Rate Prediction for Single Event Effects," *IEEE Trans. Nucl. Sci.* 39, 1577-1599 (1992).

ties of similar devices. Several methods of calculating an estimate of the upset rate exist, but the CREME suite of programs is generally recognized as a standard within the space radiation effects community, especially for comparisons between devices.[1] Using the Adams environment and the cross sections just given, the single-event upset rates behind 0.1 in. of aluminum of the CPU, PIC, and COMBO are 9.4×10^{-10}, 5.9×10^{-9}, and 1.6×10^{-6} errors/day, respectively.

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